

This Page Is Inserted by IFW Operations
and is not a part of the Official Record

BEST AVAILABLE IMAGES

Defective images within this document are accurate representations of the original documents submitted by the applicant.

Defects in the images may include (but are not limited to):

- BLACK BORDERS
- TEXT CUT OFF AT TOP, BOTTOM OR SIDES
- FADED TEXT
- ILLEGIBLE TEXT
- SKEWED/SLANTED IMAGES
- COLORED PHOTOS
- BLACK OR VERY BLACK AND WHITE DARK PHOTOS
- GRAY SCALE DOCUMENTS

IMAGES ARE BEST AVAILABLE COPY.

**As rescanning documents *will not* correct images,
please do not report the images to the
Image Problem Mailbox.**

APPLICANT: EITAN, Boaz
SERIAL NO.: 09/966,754
FILED: October 1, 2001
Page 3

AMENDMENTS TO THE CLAIMS

Please add or amend the claims to read as follows, and cancel without prejudice or disclaimer to resubmission in a divisional or continuation application claims indicated as cancelled:

1. (Currently amended) A method of fabricating an oxide-nitride-oxide (ONO) layer in a memory cell, said method comprising:

forming a bottom oxide layer on a substrate;

depositing a nitride layer; and

oxidizing a top oxide layer, thereby causing oxygen to be introduced into substantially all of said nitride layer within said memory cell, so as to restrict lateral movement of charge ~~enhance charge localization~~ within said nitride layer.

2.-3. (Cancelled)

4. (Currently amended) A method for improving the charge retention in a nitride layer of a memory cell, said method comprising:

depositing a nitride layer; and

introducing oxygen into substantially all of said nitride layer within said memory cell, so as to restrict lateral movement of charge ~~enhance charge localization~~ within said nitride layer.

5. (Currently amended) A method for improving the charge retention in a nitride layer of a memory cell, said method comprising:

depositing a nitride layer;

controlling the thickness of said deposited nitride layer; and

introducing oxygen into substantially all of said nitride layer within said memory cell, so as to restrict lateral movement of charge ~~enhance charge localization~~ within said nitride layer.

6. (Cancelled)

APPLICANT: EITAN, Boaz
SERIAL NO.: 09/966,754
FILED: October 1, 2001
Page 4

7. (Currently amended) A method of manufacturing a programmable, read only memory device, the method comprising:

forming a first oxide layer on a substrate,
forming a nitride layer on top of said oxide layer, wherein said nitride layer is 150 angstroms or less thick;
introducing oxygen into substantially all of said nitride layer within a memory cell during formation of a second oxide layer on top of said nitride layer, so as restrict lateral movement of charge ~~enhance charge localization~~ within said nitride layer;
patterning said oxide-nitride-oxide (ONO) layers into desired patterns; and
forming a gate layer over said patterned ONO layer.

8. (Previously presented) A method according to claim 7 and wherein said first oxide layer is approximately 50 – 150 angstroms thick.

9. (Previously presented) A method according to claim 7 and wherein said first oxide layer is approximately 80 angstroms thick.

10. (Previously presented) A method according to claim 7 and wherein said nitride layer is approximately 20 – 150 angstroms thick.

11. (Previously presented) A method according to claim 7 and wherein said second oxide layer is approximately 50 - 150 angstroms thick.

12. (Previously presented) A method according to claim 7 and wherein said forming said second oxide layer comprises consuming a portion of said nitride layer.

13. (Withdrawn) A programmable, read only memory device comprising:
two diffusion areas in a substrate and a channel formed therebetween;
an ONO layer at least over said channel comprising:
a first oxide layer;

APPLICANT: EITAN, Boaz
SERIAL NO.: 09/966,754
FILED: October 1, 2001
Page 5

a substantially oxygenated nitride layer having a thickness of 100 angstroms or less overlaying said first oxide layer; and

a second oxide layer overlaying said nitride layer,

said first and second oxide layers having a thickness that is the same order of magnitude as said nitride layer; and

a gate at least above said ONO layer.